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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/772,842	02/04/2004	Haruo Tanaka	10233.104USD2	5983

7590 01/18/2007  
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MINNEAPOLIS, MN 55402

EXAMINER
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MONDT, JOHANNES P

ART UNIT	PAPER NUMBER
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3663

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	01/18/2007	PAPER

**Please find below and/or attached an Office communication concerning this application or proceeding.**

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

# Office Action Summary

Application No.

10/772,842

Applicant(s)

TANAKA ET AL.

Examiner

Johannes P. Mondt

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

## Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

## Status

- 1) ☒ Responsive to communication(s) filed on 21 November 2006.
- 2a) ☐ This action is FINAL. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

## Disposition of Claims

- 4) ☒ Claim(s) 7-14 and 16-96 is/are pending in the application.
- 4a) Of the above claim(s) 10-13 and 17-96 is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 7-9, 14 and 16 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

## Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on \_\_\_\_\_ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
- Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

## Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some \* c) ☐ None of:
- ☐ Certified copies of the priority documents have been received.
  - ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
  - ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

## Attachment(s)

- |  |   |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892)            | 4) <input type="checkbox"/> Interview Summary (PTO-413)           |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)   | Paper No(s)/Mail Date. _____                                      |
| 3) <input checked="" type="checkbox"/> Information Disclosure Statement(s) (PTO/SB/08) | 5) <input type="checkbox"/> Notice of Informal Patent Application |
| Paper No(s)/Mail Date <u>10/27/06</u> .  | 6) <input type="checkbox"/> Other: _____                          |

## **DETAILED ACTION**

### ***Continued Examination Under 37 CFR 1.114***

A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 11/21/06 has been entered.

### ***Information Disclosure Statement***

The examiner has considered the items listed on the Information Disclosure Statement filed 10/27/06. A signed copy of Form PTO-1449 is herewith enclosed.

### ***Response to Amendment***

Amendment filed 11/21/06 with said RCE forms the basis for this office action. Applicant substantially amended all elected claims 7, 8, 9, 14 and 16. Comments on Remarks including not only those submitted with said RCE but also those submitted 10/23/2006 prior to said or any Amendment after final rejection are included below under "Response to Arguments".

### ***Claim Objections***

1. **Claims 7-9, 14 and 16** are objected to because of the following informality: the wording "and abut each" (line 6 of claim 7) should be replaced by: "abut each". Appropriate correction is required.

***Claim Rejections - 35 USC § 103***

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

1. ***Claim 7*** is rejected under 35 U.S.C. 102(e) as being unpatentable over Wu et al (6,031,856) in view of Mai et al (JP Patent JP410021578 A).

*Wu et al teach* a surface-light-emitting device 24 (Figure 2, col. 2, l. 31 – col. 4, l. 25; for 26 see col. 2, l. 55) including a luminescent layer (inherent in VCSEL 26 (col. 2, l. 50 and l. 54) as in any semiconductor laser is a light-emitting layer that emits light when subjected to a voltage, i.e., a luminescent layer, because the driving force of lasing is recombination of electrons and holes accelerated towards each other, the acceleration mechanism being provided by an electric field) and an electrode structure (also inherent in said VCSEL as it is inherent in any semiconductor laser because the electric field is created by means of a voltage difference, and hence two different voltages must needs be provided to the areas abutting the luminescent layer through an electrode structure, i.e., highly conductive terminal), the luminescent layer emitting light as a result of applying a voltage to the electrode structure (inherent, see above), wherein a shielding layer 32 (col. 2, l. 49-53, being “partially reflective”, hence shielding light) formed in a shape substantially corresponding to a pattern of

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interference fringes of a hologram, i.e., said shielding layer is the layer in which said hologram is produced, is provided at a position outside of the luminescent layer (32 is outside VCSEL 26 hence *a fortiori* outside said luminescent layer, said luminescent layer being inside said VCSEL 26), and wherein the light from the luminescent layer is emitted through the shielding layer 32 (col. 2, l. 55-58).

*Wu et al do not necessarily teach the limitation that said shielding layer and said luminescent layer to abut.*

*However, it would have been obvious to include said limitation in view of Mai, who, in a patent on a surface light-emitting device (surface emitting laser (Drawing 2) integrated with a hologram (see abstract, "Problem to be Solved"), hence analogous art, teach said laser diode 12, which inherently is a luminescent layer, and said hologram 14 to abut (see Drawing 2). Examiner takes official notice that compact, integrated design in the semiconductor art has long been recognized to yield both cost and reliability advantages.*

2. **Claims 8, 9, 14 and 16** are rejected under 35 U.S.C. 103(a) as being unpatentable over Wu et al and Mai as applied to claim 7 above, and further in view of Kozlov et al (6,160,828, cited in previous action).

*On claims 8, 9 and 14: As detailed above, claim 7 is unpatentable over Wu et al in view of Mai. Wu et al nor Mai necessarily teach the further limitation as defined by claims 8, 9, or 14.*

*With regard to claims 8 and 14, it would have been obvious to include said further limitations as defined in claim 8 in view of Kozlov et al, who, in a patent on a*

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vertical; cavity surface emitting laser (VCSEL) (Figure 5, title, abstract, and cols. 5 and 6), hence analogous art, teach a pair of electrode layers 120 and 121 (col. 5, l. 65 – col. 6, l. 3) interposing the luminescent layer 110 (col. 5, l. 52-61) therebetween, and wherein one of the electrode layers (either one of 120 and 121, say 120) is formed as a transparent electrode layer (loc.cit.), with the light generated by the luminescent layer emitted in a direction substantially perpendicular to the luminescent layer as a laser beam after carrying out lasing through resonance (thus meeting also claim 14 as a result). Because the shielding layer by Wu et al is provided outside the VCSEL said shielding layer is a fortiori provided outside said one electrode layer also in the combination of the invention by Wu et al and the teaching on Kozlov et al. on the electrode structure.

*Motivation* to include the teaching by Kozlov et al derives from the advantage of achieving maximum surface area of the luminescent layer to be active at minimal voltage difference (because of their short relative distance) between the electrodes. Examiner herewith takes official notice that this motivation is the reason why VCSELs are almost if not always constructed in this manner.

*On claim 9:* It would furthermore have been obvious to include the limitation as defined by claim 9 also in view of Kozlov et al, who teach a supporting member 113 having transparency (col. 5, l. 48-52) provided to a position inside the VCSEL; in the combined invention this position is outside of the shielding layer 32 (namely: outside the VCSEL 26), and wherein light from the luminescent layer is emitted through said one electrode layer 120 and the supporting member (see Figure 5; loc.cit; see also col. 4, l.

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20-25), and , in the combined invention, through the shielding layer 32. *Motivation* to include the teaching by Kozlov et al in the invention by Wu et al in this regard derives from the advantage of transparency of material when light emission must occur through light transmission through the medium made of said material. In particular, if the supporting member 113 were not transparent light would be absorbed and the light efficiency would be poor if at all finite.

*On claim 16:* although Wu et al do not necessarily teach the further limitation as defined by claim 16, it would have been obvious to include said further limitation in view of Kozlov et al, who teach to include in the VCSEL 26 a plurality of reflecting mirrors (DBRs 111 and 112; see col. 5, l. 50-61 and col. 4, l. 1-24) each having a reflective plane substantially parallel to the luminescent layer 110 (see Figure 5), wherein the reflecting layers resonate the light generated by the luminescent layer in a direction substantially perpendicular (namely in the emission direction, which is perpendicular to the plane of 110; see Figure 5) to the luminescent layer.(as each reflect a substantial amount of light a substantial amount of light reflected by one DBR is also reflected by the other DBR and hence "resonate" is met and is also a necessary condition for lasing; see, e.g., Fukuda, M., "Optical Semiconductor Devices", pages 165-167). *Motivation* to include the teaching by Kozlov et al in the invention by Wu et al derives from the resulting controllability of the output spectrum (col. 4, l. 8-10).

### ***Response to Arguments***

Applicant's arguments filed 11/21/06 and 10/23/06 have been fully considered but they are not persuasive.

As a preliminary matter the wording "and abut each other" (lines 6-7 of claim 7) is objected to and should be replaced by "abut each other". See objections under "Claim Objections" above. The problem clearly is nothing more than a typographic error, because, as witnessed by Remarks filed 10/23/06, the intent clearly is to recite that said shielding layer and said luminescent layer are to abut each other.

The new claim language is found unpatentable over Wu as cited in view of Mai (JP 08-174702), who teaches laser diode and hologram to abut in a single integrated, i.e., unitary structure called laser diode hologram unit (LDHU). Examiner takes official notice that compact, integrated design in the semiconductor laser art has long been recognized to yield both cost and reliability advantages. Therefore, motivation to include the teaching by Mai in the invention otherwise defined by Wu exists. The rejection overleaf were prompted by these considerations.

### ***Conclusion***

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Johannes P. Mondt whose telephone number is 571-272-1919. The examiner can normally be reached on 8:00 - 18:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jack W. Keith can be reached on 571-272-6878. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.




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Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

JPM  
January 5, 2007

Patent Examiner:

  
Johannes Mondt (Art Unit: 3663)